A 8 WATT HIGH EFFICIENCY C BAND POWER AMPLIFIER

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ABSTRACT

A 8 Watt C-band power module is reported. This power amplifier comprises two power MMICs combined in parallel and balanced between two Lange couplers on alumina substrate.

At 25°C, an average power amplifier delivers a saturated output power higher than 38.5 dBm, with an associated gain of 14 dB and a power added efficiency higher than 27%, over the 5 GHz - 6 GHz bandwidth, under DC and RF pulse conditions. The best power amplifier exhibits the following performances : a saturated output power higher than 39 dBm, a gain of 15 dB, and an associated power added efficiency of 31 %.

Keywords : MMIC, power amplifier, high efficiency.

1 - INTRODUCTION

In recent years, many C-band power amplifiers were realized for various applications including transmitter modules for phased array antennas (refs 1-5). For such applications, in addition the obvious requirements of power and gain, key constraints to driving the development of these amplifiers are high power efficiency, low DC consumption, and size.

Various approaches to meeting these requirements, have been reported over the last several years. One approach employs compact, two-stage MMIC which incorporates the interstage and partial input matching circuitry on-chip, while using low loss off-chip components to power match the output and complete the input matching. This approach (refs 2) has produced some of the best performances : at 2 dB compression, a minimum 35 dBm output power is measured under CW conditions, with a 18 dB associated gain and 32 to 36 % power added efficiency. Alternative approach involving fully matched on-chip MMIC in which all matching is incorporated on-chip has also been presented. A five company transfer of design and process of a C-band 3 Watt 2-stage amplifier is summarized in ref.1 : an average output power of 34 dBm with a 15 dB gain and 18 to 22 % power added efficiency is obtained under 11 % RF duty cycle pulse conditions. A slightly better efficiency of 22-24 % was obtained in ref. 3 with CW conditions but for lower drain bias (7.8 V). Last results from Thomson Composants Microondes (ref. 5) reported a 36 dBm output power (at 3 dB compression), with a 18 dB associated gain and 23 - 26 % power added efficiency, measured under 10 % duty cycle pulse condition and a drain bias of 10 V. With a drain bias of 7 V, power added efficiency increases up to 32-37 % with a 35 dBm output power.

This paper describes the design and the performances of a power amplifier which comprises two identical fully on-chip matched MMICs presented in ref. 5.

2 - AMPLIFIER DESIGN

2.1 - MMIC design

The MMIC was designed to deliver a minimun saturated output power of 3 Watt (ref. 5). The gate width of this monolithic amplifier was optimized for a given power objective over temperature range (ref. 6). To meet the requirements, the topology chosen is a two-stage, symmetrical arborescent amplifier with full on-chip matching networks (input, interstage, output).The output stage consists of four 1760μm wide FETs driven by two 1230μm wide FETs. The on-chip output matching network was optimized so that optimum power load impedances are presented to the output FETs. As the amplifier works in saturation, the first stage was also optimized to provide high output power rather than to achieve a flat gain. The chip size is 4.5 x 2.5 mm^2 (figure 1).

2.2 - Module design

Two MMICs combined in parallel are balanced between two Lange couplers on alumina substrate. The MMICs and the couplers are mounted on Molybdenum carrier. This power module also incorporates DC blocking and DC bias circuitry, so that the drain voltage supply is set at 9V and the gate voltage at -5.5V. The total size of the module is 12.45 x 6.85 mm^2, and the layout is shown in figure 2.

3 - TECHNOLOGICAL PROCESS

The monolithic circuits were fabricated at Thomson Composants Microondes using the standard HP07 process. Selective N and N$^+$ ion implantation is employed to form the MESFET structure. After formation of ohmic contacts, the Schottky barrier gates are formed using electron beam lithography (gate length = 0.7μm). A first level metal interconnect is deposited for interconnection and capacitor bottom plates. Silicon nitride dielectric used for the MIM capacitors is then deposited followed by the second metal level which constitutes the capacitor top plates and the other components such as spiral inductors, as well as transmission lines. The next step is a level of plated metal that realizes air bridge interconnects. The substrate is thinned, via holes etched, the back side metallized and the wafer separated into individual MMICs.

4 - MEASURED PERFORMANCES

4.1 - MMIC measurements

Figure 3 shows typical results of on-wafer power measurements of the amplifiers: 16 out of 32 amplifiers exhibit an output power higher than 36 dBm and a 18 dB gain for an input power of 18 dBm (3 dB compression) over the bandwidth, which gives an on-wafer power yield of 48%. The test conditions are the following: drain bias and RF power are pulsed, the RF pulse length used is 10μs, drain pulse length is 15μs with a 3% duty cycle pulse. During these on-wafer measurements, average values of drain current and power added efficiency were recorded: Ids = 1.3A, and PAE = 30%.

Some amplifiers were mounted on a test fixture and were measured under 10% duty cycle pulse condition. For power performances, the circuits were biased at 10V drain voltage and at a drain current near Idss/2 (gate bias = - 2V). Output power is 36 dBm with a 25% power added efficiency. Figure 4 shows the performance of three circuits mounted on a test fixture.

4.2 - Module performances

At 25°C, an average power module delivers a saturated output power higher than 38.5 dBm, a 14 dB associated gain and a power added efficiency higher than 27% from 5 to 6 GHz (figure 5). These results were measured under DC and RF pulse conditions, with a 10% RF duty cycle and an input power of 24 dBm. At 65°C, the output power decreases to 37.5 dBm, under the same measurement conditions. The best performances are presented in figure 6: a saturated output power higher than 39 dBm, a gain of 15 dB, and a power added efficiency of 31% are achieved.

5 - CONCLUSION

The C-band power amplifier based on the use of two fully on-chip matched power MMIC balanced between two Lange couplers on alumina described in this paper demonstrated an output power ranging from 6 to 8W with a gain of 14 dB and power added efficiency ranging from 27 to 31%. These results were obtained under DC and RF pulse conditions with a 10% RF duty cycle.

These performances demonstrate the ability offered by monolithic technology to achieve a 30% power added efficiency module for high output powers.

ACKNOWLEDGEMENTS

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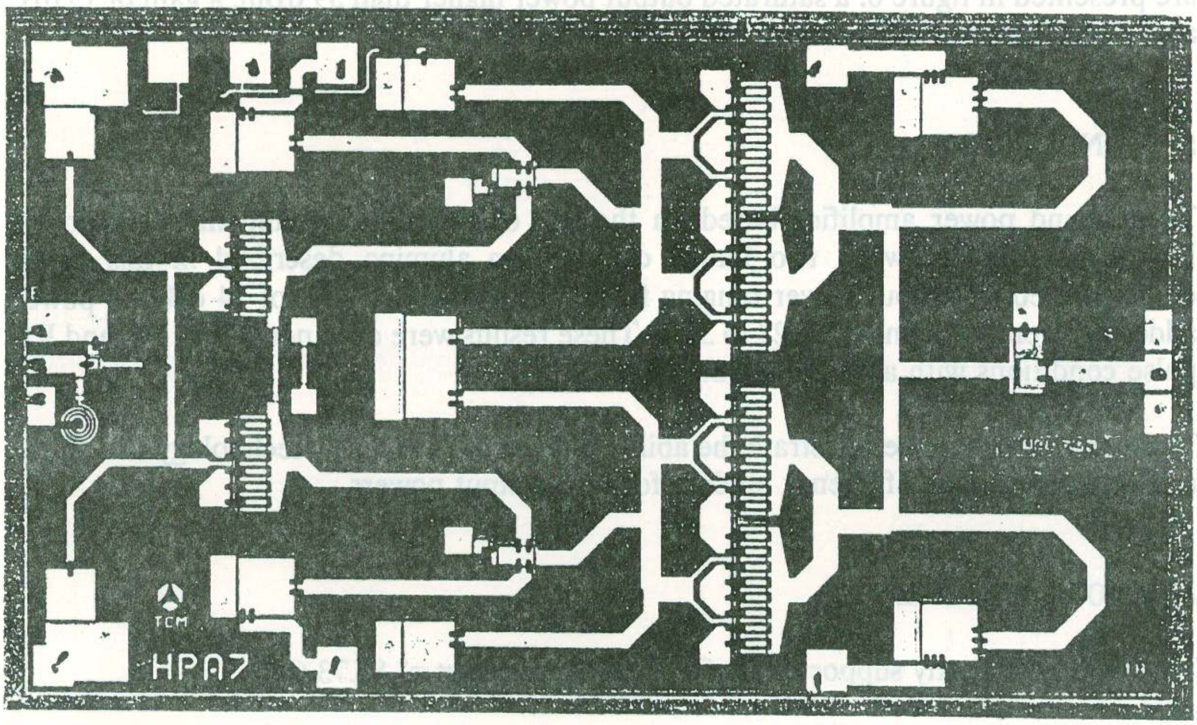


Figure 1 : *Photograph of monolithic amplifier.*

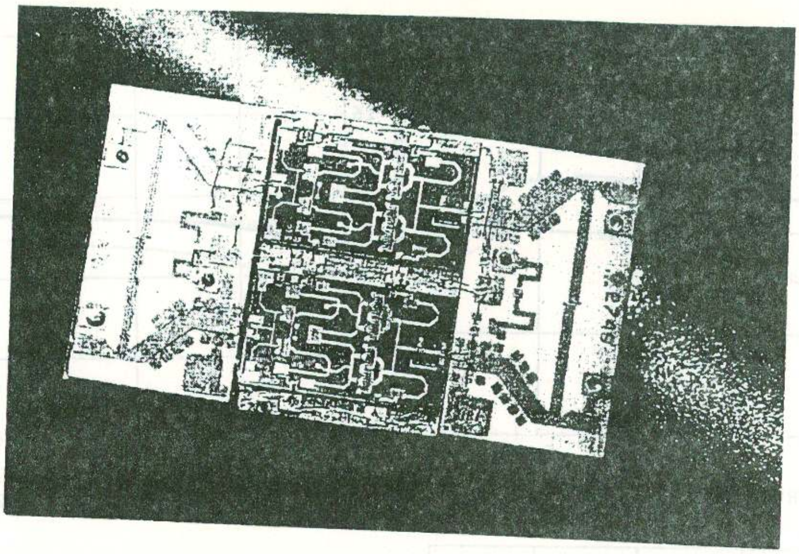


Figure 2: *Photograph of the module.*

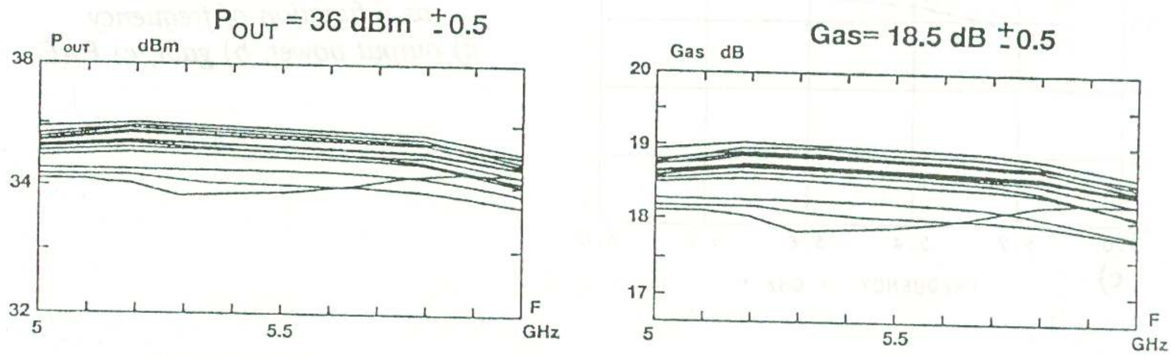


Figure 3: *Results of on-wafer power measurements of the monolithic amplifier.*

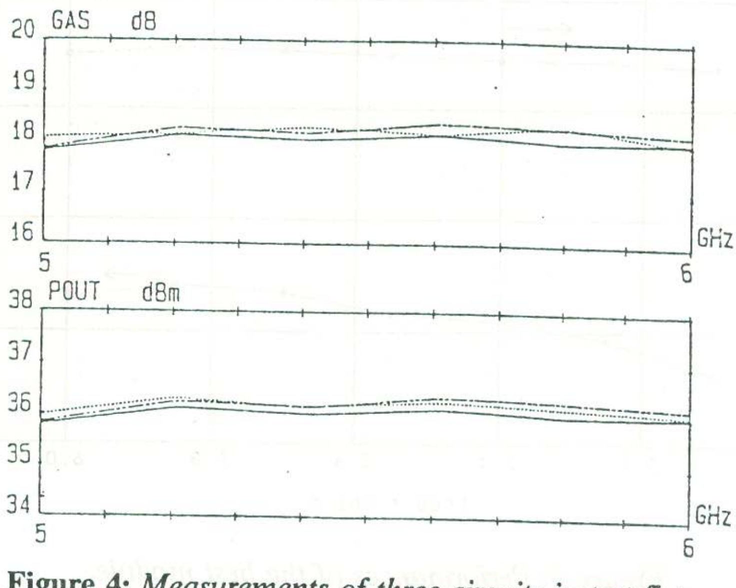
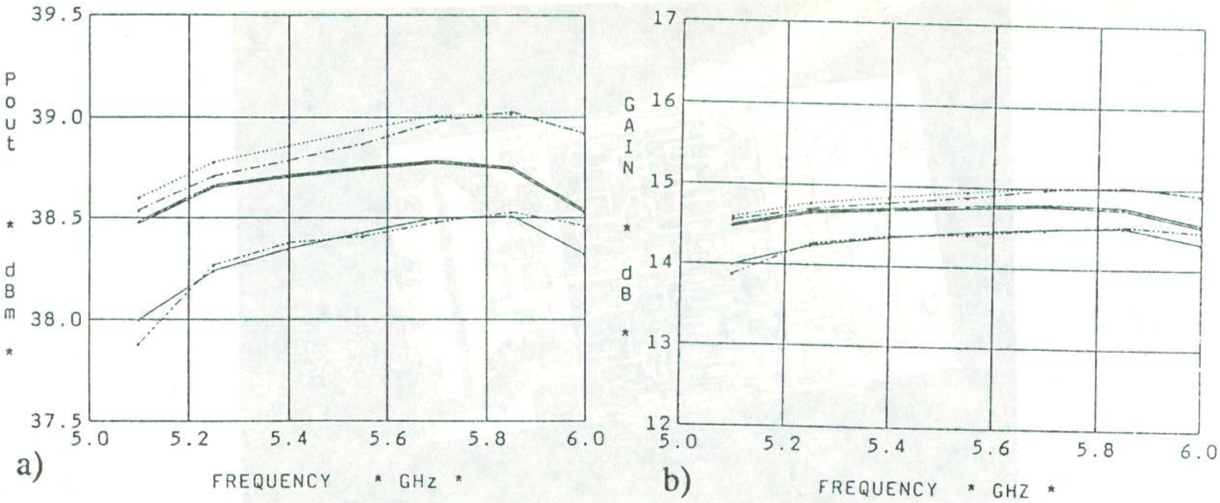


Figure 4: *Measurements of three circuits in test fixture.*



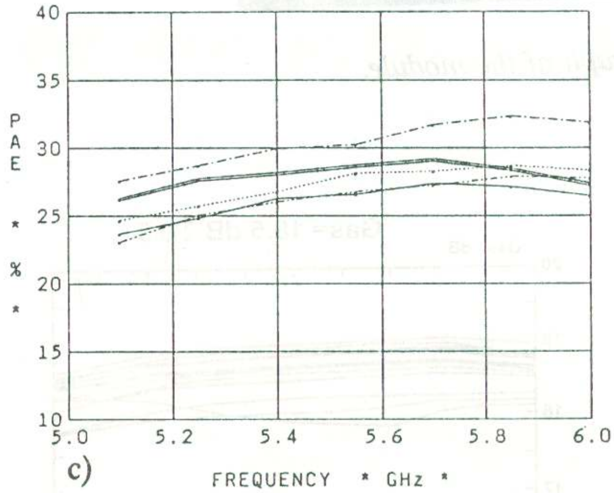


Figure 5: *Power performances of 5 modules as a function of frequency a) output power, b) gain, c) PAE*

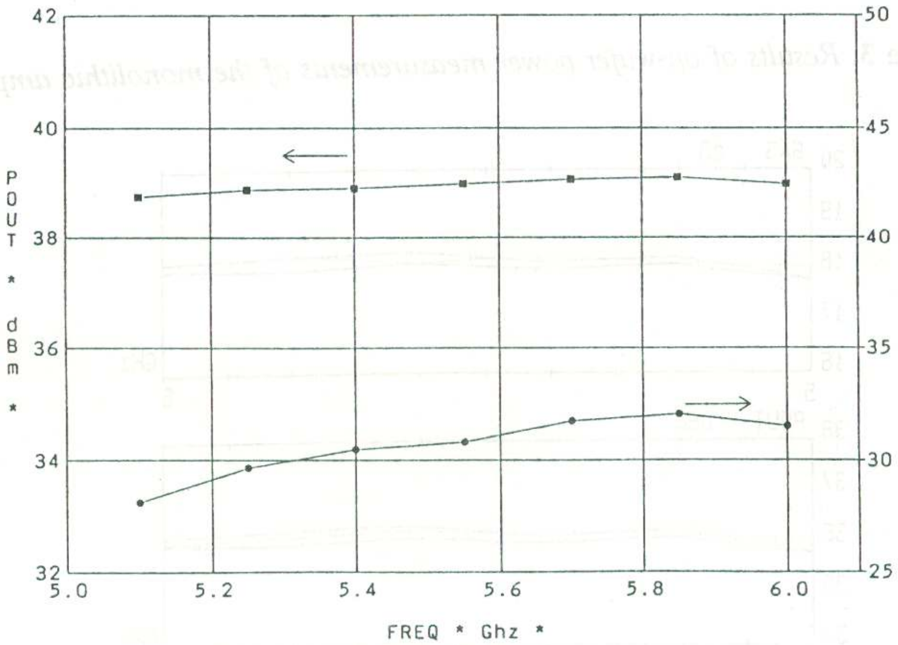


Figure 6: *Performances of the best module.*